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SINE OUTPUT DDSs A SURVEY OF THE STATE OF THE ART

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Abstract

This paper presents a survey of the latest techniques and hardware advances in sine output direct digital synthesizers (DDSs).

First, a brief description of the theory of sine output DDSs is presented. A sine output DDS has the advantage of being able to synthesize high spectral purity sine wave signals over a wide range of frequencies utilizing compact digital integrated circuits containing an accumulator, a sine look-up table, and a digital-to-analog converter (DAC). (The DDS is completed with an output filter.) The DDS can produce an output frequency from zero to a maximum frequency that is on the order of 1/3 of the clock frequency of the digital components. The principal advances in DDSs have been in increasing the maximum frequency (clock speed) and in increasing the spectral purity (spur reduction).

Second, sine output DDS designs are examined that fall into two broad categories: designs for high speed and spectrally clean performance and designs for applications that require special features. Results are presented showing how the spectral purity of the DDS is related to the complexity and performance parameters of the digital components. Recent advances in architectural techniques are described that are designed to optimize spectral performance while minimizing architectural complexity.

Finally, a survey of the latest DDSs and components developed by several manufacturers are described presenting key performance parameters such as clock speed, spectral purity, frequency resolution, DC power consumption, and special features. A plot of reported spurious performance on DDSs (or DACs for DDSs) is presented revealing a performance barrier that designers are striving to break. The advances necessary to break this barrier will be discussed.

Introduction

Sine output direct digital synthesizers (DDSs) digitally generate a stepped sine wave at an output frequency f_o from a clock frequency f_c (figure 1). These DDSs have been in use since the late 1960s [Gillette, 1969] and have become more and more popular as digital logic has advanced in complexity and performance. Sine output DDSs are not the only type of DDSs [Reinhardt, 1985], but have become the most widely used because of their high spectral purity and all digital implementation. This paper surveys the latest developments in the state of the art of sine output DDSs and discusses the direction of future advances. To simplify terminology in the remainder of this paper, we will refer to sine output DDSs as DDSs with the implication that we are discussing only the sine output type.

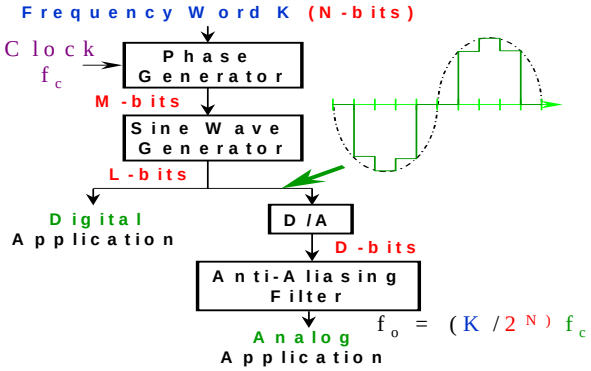

Figure 1. Conceptual Block Diagram of a (Sine Output) DDS. The analog application requiring the DAC is the focus of this paper as both the digital and DAC imperfections are discussed.

In addition, three techniques for the digital generation of a sine output are shown in figure 2. The digital signal processor (DSP) computes the sine output but is typically slow compared to the DDS. The waveform generator reads sine-output data from previously written random access

memory (RAM). This technique is widely used in test equipment for radar and communications applications. The scope of this paper is limited to the accumulator based sine-output DDS.

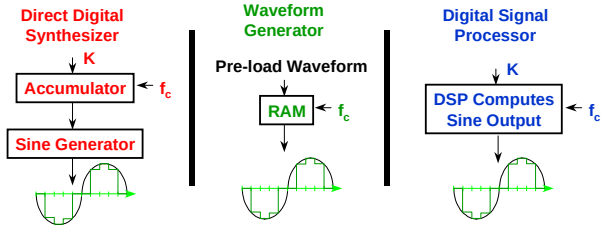

Figure 2 Three methods for the digital generation of sine output wavefroms are shown. The DSP is typically slow. The waveform generator is widely used in test equipment pattern or arbitrary waveform generators in radar and communications applications. The phase accumulator followed by a sine generator (phase-to-amplitude translation) based DDS is the focus of this paper.

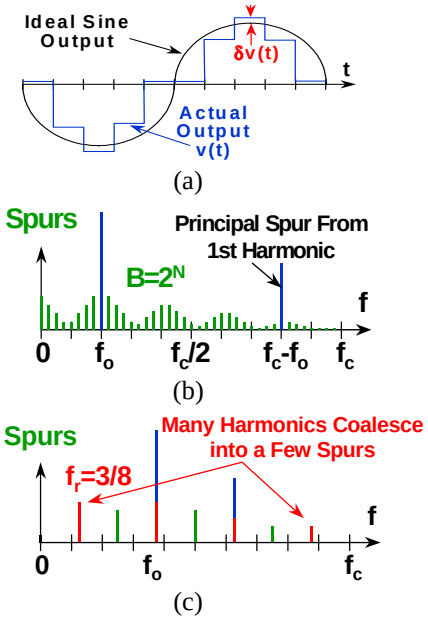

Figure 3. (a) The uniformly stepped output is periodic with period B (b) The Fourier harmonic expansion due to the perodicity of B results in B spurs from frequency 0 to F_c. The non-ideal sine wave also has a Fourier harmonic expansion. Aliasing moves these spurs from the harmonic locations to the B locations. (c) However, for the normalized frequency (Fr =K/B), when K and B are not relatively prime, the fraction is written as an irreducible fraction (i.e. 3/8), and the multitude of B spurs are coalesced into a few spurs as shown. An in-depth derivation is given by [Reinhardt, 1985].

The conceptual block diagram of a (sine output) DDS shown in Figure 1 consists of two components, a phase generator and a sine wave generator. The phase generator is driven by a clock frequency f_c. At the n^{th} clock period, the phase generator increments the phase ϕ_n by an amount given by

$$\Delta\phi = 2\pi\frac{K}{2^N}$$

where K is an N-bit frequency word. Since this occurs at the clock rate, the phase steps through 2π radians at a frequency

$$f_o = \frac{K}{2^N} f_c = F_r\ f_c$$

ϕ_n is then truncated to M-bits and sent to the sine wave generator, which generates an L-bit digital word proportional to $\sin(\phi_n)$.

If the DDS is utilized in a digital application as part of a larger digital signal processor, the DDS is complete as described. If an analog output is required, a digital-to-analog converter (DAC) and an anti-aliasing filter are required to complete the DDS. The DAC takes the sine output word truncated to D-bits and converts this into a stepped voltage as shown in Figure 1. The anti-aliasing filter, whose low pass knee is below $f_c/2$, is required to smooth the output to improve the spectral purity. According to the Sampling Theorem, a perfect sine wave with no phase jitter is recovered, if the process of generating the stepped sine voltage output were perfect.

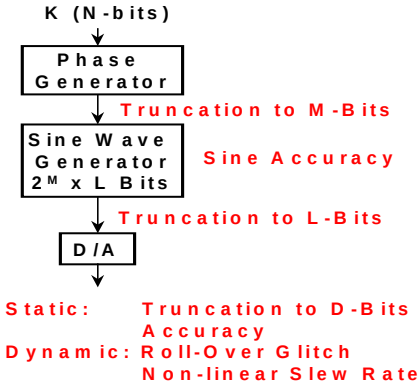

Figure 4. Some static errors are due to word length truncations in the DDS and DAC, and some dynamic errors are due to the roll-over glitch and non-linear slew rate. An in-depth description of how to linearly slew the DAC response is given by [Essenwanger, 1998].

Imperfections in the sine generation process cause spurious outputs to be generated (figure 3). Because of the uniform sampling process involved, these imperfections can be aliased down to low frequency offset spurs, which can be as close as $2^{-N}f_c$ from the carrier [Reinhardt, 1985]. These imperfections are caused by several factors [Reinhardt, 1985]. First, the truncation of the phase word to M-bits, the sine generation accuracy and truncation to L-bits cause imperfections in the sine output. Second, DAC

imperfections, which can be classed as static and dynamic imperfections, also cause spurs (figure 4). The static imperfections are due to the D-bit truncation of the DAC word and the static inaccuracies of the DAC. Dynamic imperfections are largely due to the non-linear slew rate of the DAC [Essenwanger, 1998] and the fact that all the bits of a DAC don't switch at the same time, causing a glitch as the input word is changed (glitch area). Spur levels are generally given by 6 dB per bit of accuracy, though the DAC imperfections can generate spurs at the 7-8.5 dB per bit level [Garvey, 1990]. The reader is referred to [Reinhardt, 1985] for an in-depth derivation of the harmonic aliasing of spurious frequencies in DDS.

The 6-dB per bit rule-of-thumb is valid when the aliased spurious power is coalesced into one spur [Tierney, 1971] or summed. The coalescing into a few spurs is shown in figure 3c, but the summation of spurious power may also be computed for all output frequencies F_o as shown in figure 5, where all spurs are summed up to $f_c/2$ or 200MHz for this example. At F_o=1/4 f_c (100MHz) there are no spurious. At F_o=1/8 f_c and 3/8 f_c worst case spurious results.

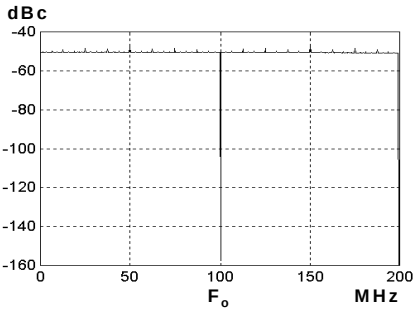

Figure 5. The root-sum-square of spurious power as a function of output frequency [Essenwanger, 1996]. The response is searched for worst case start phase and post-compensated for sinc(πF$_r$)sinc(πF$_r$Δ) [Essenwanger, 1998].

The RSS of spurious is based on the following equation [Essenwanger, 1996], after "total integrated spurious" [Kent, 1995]:

$$\mathrm{RSS}_{\mathrm{Spurious}} = 20\log\left\{\frac{\sum_{i=1}^{i<Nyquist}(Cm_i)}{Cm_0}\right\}^{1/2}$$

where $\boldsymbol{Cm_i}$ = magnitude of power. i = 0 for the fundamental. i = 1,2,3,…,(<Nyquist Rate) for spurious, excluding the alias. The approximate variance power of the errors for a uniform quantizer is well known [Rabiner, 1975], [Colotti, 1990] as
where q is the quantization. Thus, for uniform quantization of a sine wave

$$E(\varepsilon^2) = \frac{q^2}{12}$$

$$noise\,|_{rms} \approx \sqrt{E(\varepsilon^2)} = \frac{q}{\sqrt{12}} = \frac{1}{\sqrt{12}} \text{ for } q \text{ normalized}$$

$$signal\,|_{rms} = \frac{2^k}{2\sqrt{2}}$$

$$SNR = 20\log\left(\frac{signal}{noise}\right) = 20\log\left(\frac{\frac{2^k}{2\sqrt{2}}}{\sqrt{12}}\right)$$

$$= 20\log\left(2^k\right) + 20\log\left(\frac{\sqrt{6}}{2}\right)$$

$$\approx 20\log\left(2^k\right) + 1.761 = 20\log\left(2^8\right) + 1.7609 \quad \text{for an 8 - bit DAC}$$

$$\approx 48.1 + 1.8 = 49.9 \text{ dB}$$

This result, in close agreement with the typical level shown in figure 5, confirms the practical usefulness of the 6 dB per bit rule-of-thumb (the 1.8dB constant is understood). The root-mean-squared (RMS) was also studied instead of the RSS with similar results, except the RMS had slightly more variations (not as smooth) as shown in figure 5.

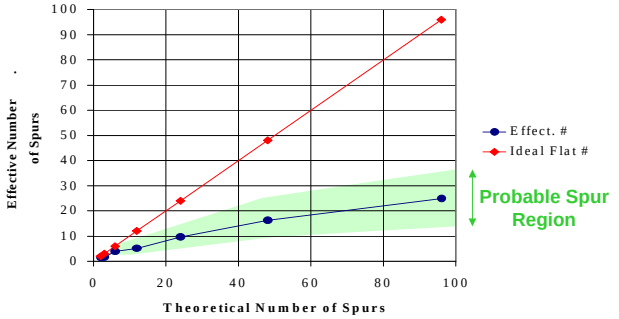

Figure 6. The effective number of dominant spurs is reduced from the theoretical spectrally flat number by the coalesced spurs for DDSs.

In figure 6, most of the power is divided among the fewer dominant coalesced spurs. For the ideal flat spurious spectrum case, the spurious power is evenly divided among all spurs. The 6 dB/Bit rule-of-thumb is approached as the two curves converge and approach the one spur assumption near the chart origin.

DDS Survey

Table 1 shows various phase-to-sine conversion architectures (or DDS back-end circuitry) for which Vankka has simulated worst case spurious (algorithm error) [Vankka, 1998]. Raytheon's back-end (BE) architecture is appended to the bottom of the table as well as the unmodified Sunderland BE. It is difficult to compare architectures when new unconventional methods of performance are used without all parameters and

conditions defined. The Vankka worst case spur was reported to be simulated for the Nicholas phase accumulator. Because it is not clear all of the conditions for the simulations, the same data is not available for the Raytheon DDS; however, the unmodified Sunderland architecture is 12-bits +/- 2 LSBs which has a worst case spur of nearly 61.8dBc by the 6dB/Bit + 1.8dB rule-of-thumb. Sunderland reports measured performance for Fr=3/8 of 65.4dBc [Sunderland, 1984]. Simulations with an ideal DAC model for Fr=11/32 gives -67dBc [Essenwanger, 1987] (without a search routine for the worst-case start phase).

Table 1. Modified Vankka's Table [Vankka, 1998]: updated with the Raytheon [2] and unmodified Sunderland [26] Direct Digital Synthesizer Back-End Sine-Output Architectures.

Architecture	ROM Required [bits]	Compression Ratio	Significant Additional Logic Circuits	Worst Case Algorithm Error [dBc]	Comments
Uncompressed ROM	2^{14} x 12	1:1	(none)	-97.23	reference
Modified Sunderland	2^8 x 9 2^8 x 4	59:1	adder	-86.91	good spur level and simple
Nicholas Fine Linear Interpolation	2^8 x 9 2^8 x 3	128:1	adder/subtract	-88.94	best compression ratio
Conventional Taylor Series Approximation	2^7 x 14 2^7 x 9 2^5 x 3	64:1	2 adders, multiplier	-97.04	conventional multipliers are slow
Cordic	(none)	N/A	14 pipelined stages, 18-bits wide	-84.25	slightly more circuitry needed, AM possible
Raytheon's Taylor Series Approximation	2^7 x 14 2^7 x 11 2^5 x 7	67:1 (w.r.t. 2^14x13 ROM)	multiplier, multiplexer, adder	13-bits $^+/_-$ 1-bit	optimized for performance, and cell reuse from a sine and cosine output capable design
Unmodified Sunderland	2^8 x 11 2^8 x 4	51:1	adder	12-bits $^+/_-$ 2-bits	simple

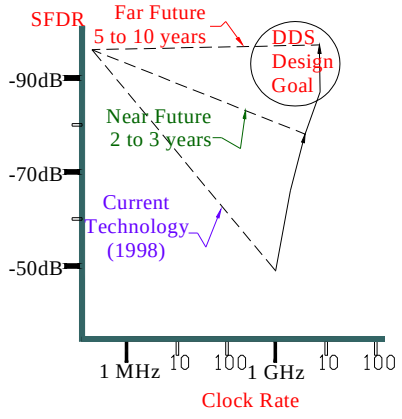

Figure 7. DDS Technology Trends. The DDS Design Goal is High SFDR and High Speed to get Wide Bandwidth such that signals can be synthesized at IF. The Current Technology, Near Future, and Far Future Expectations are Shown [Estrick, 1995].

Vankka also reports that the modified Sunderland is 14 dB better than the unmodified Sunderland. Thus, the Vankka simulation for the unmodified Sunderland DDS should be about 14-86.91= -72.91dBc. Hence, there is about an 11dB discrepancy from worst case spurious predictions by the rule-of-thumb for the conventional Sunderland architecture and about a 6dB discrepancy (or more) from simulations. See [Sunderland et al., 1984] for a conventional calculation of DDS algorithm truncation in terms of signal-to-noise ratio. On the other hand, the Raytheon DDS performance is equivalently 13-bits +/- 1 LSB or the equivalent of a 12-bit linear DAC with nearly ideal phase-to-sine conversion, similar to what a full ROM BE would provide (approaching the -97.23 dB performance as read from Vankka's table).

The trends and design goal of DDS technology are shown in figure 7. By innovative circuits and higher speed IC processes, the goal should be attainable within about 10 years.

The survey results are shown in table 2 and figures 8 and 9. Because of the limited number of parts that can reasonably be shown on one chart, the list is not exhaustive. However, this is representative of the state-of-the-art in DDS.

Figure 8 shows the lower output frequency capable DDS (and DACs useful for DDS). These are the state-of-the-art for high resolution DDSs and are often used along with conventional direct and indirect synthesizers for wide bandwidth and synthesis at IF frequencies. Figure 9 shows the high speed (wide bandwidth) capable DDSs (and DACs) and reveals a barrier in performance, as the lower right corner of the chart is clear. This barrier is attributed to the high-speed performance limitations of the DAC.

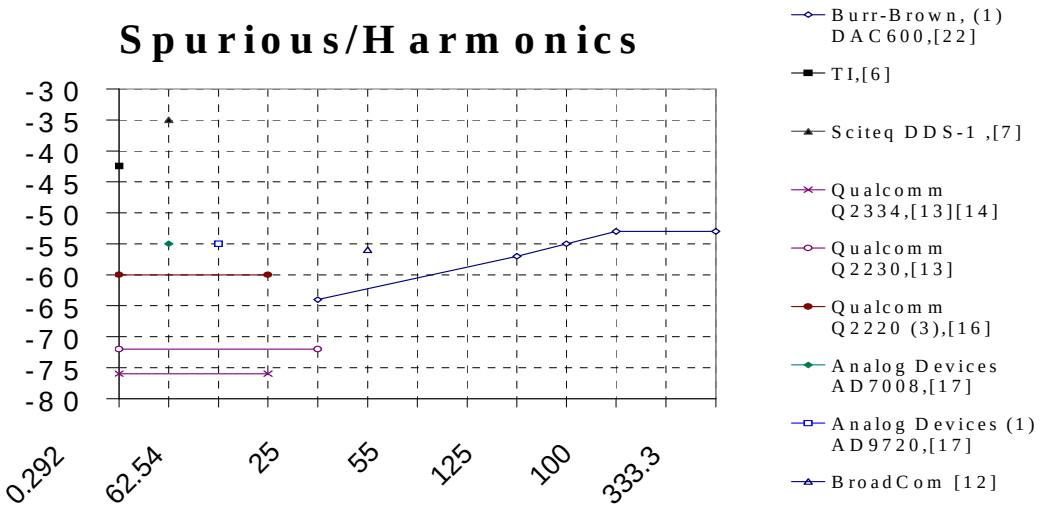

Figure 8. The Survey Results for Lower Bandwidth DDSs and DACs useful for DDS. While the list is not exhaustive, it is representative of typically commercially available and state-of-the-art prototype technology found in the literature [31].

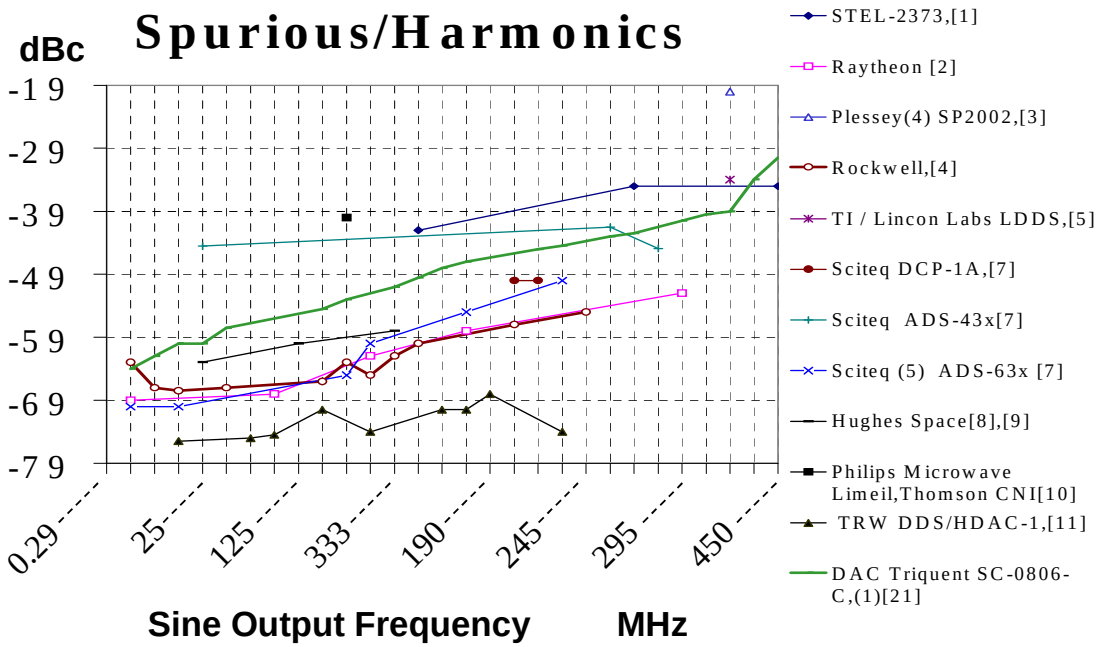

Figure 9. The survey results for high-speed DDSs and DACs useful for DDS. The lower right corner of the chart is clear of data points revealing a barrier in performance attributed to the DAC's high-speed performance limitation. The table captures the data to the authors' best ability in interpreting the published information [31].

Notes for Table 2 and Figures 8 and 9:

(1) DAC useful for DDS application.
(2) Has noise reduction circuit that manufacturer shows reducing discrete spurious from -57dBc to -72 dBc for approximately a 4 MHz output frequency.
(3) The Q0320-1 DDS synthesizer card includes the Q2220 DDS and Sony CXD1171M DAC.
(4) Internal divide-by-two cuts effective clock to half.
(5) Uses Triquint's GaAs 14-bit DAC.
(6) The reported typical SNR is about 6dB worse than the plotted "Peak Harmonic" for the 1st Image. It is unclear if the technique of [Hill,1993] is suggested.
(7) Some manufacturers distinguish between spurious and harmonics (e.g. Sciteq or Osicom), but often this distinction is not made clear.

Table 2. Survey of DDS/DAC Features [31]

Identifier	Clock Rate MHz (max)	Frequency Resolution	Result Word(s) or DAC-bits	LFM Out	Phase Offset	I/Q Out	Tech - nology	Power Diss	Package
STEL-2373,[1]	1000	20.8023 Hz	8	no	2-bit	no	GaAs	12 W	2"x1" hybrid
Raytheon [2]	1000	0.232 Hz	13	yes	32-bit	no	Bipolar	7.5 W	IC/Module
Plessey(4) SP2002,[3]	1600	0.5 Hz	8	no	no	yes		6 W	monolithic IC
Rockwell,[4]	500	28-bits	12	no	8-bits	no	GaAs HBT	5.5 W	1.12"x2.33"x0.2" hybrid
TI / Lincon Labs LDDS,[5]	800	32-bits	10						
TI,[6]	450	28-bits	8	yes	no	yes	GaAs HBT		monolithic IC
Sciteq DCP-1A,[7]	700	24-bits	12	yes	12-bit	no		15 W	1.2"x5"x7.8" module
Sciteq VDS-8,[7]	20	32-bits BCD 0.1 Hz exact	12	no				3W	1.2"x7.8"x5" module
Sciteq DDS-1,[7]	25	32-bits	12	no	16-bit	no	CMOS	1.57W	Hybrid/ 74-pin LCC
Sciteq ADS-43x[7]	1600	30-bits	8		no	yes (6)	Silicon	6W/8W	
Sciteq (5) ADS-63x [7]	500		14		4-bits		GaAs		
Hughes Space[8],[9]	1000	22	12	no	no	no	InP HBT		IC
Philips Microwave Limeil, Thomson CNI[10]	1250	25-bits	12	yes	no	no	GaAs MESFET	2.2W	6 ICs
TRW DDS/HDAC-1,[11]	500	24-bits	12	no	no	no	HBT GaAs		1.4 cubic in.
BroadCom [12]	800	32-bits	12	no	12-bits	yes		3W + DAC	IC

(Table 2 Continued)

Identifier	Clock Rate MHz (max)	Frequency Resolution	Result Word(s) or DAC-bits	LFM Out	Phase Offset	I/Q Out	Tech - nology	Power Diss	Package
Qualcomm Q2334,[13][14]	50	32-bits	12	no	3-bits	yes		0.67W	68-pin PLCC
Qualcomm Q2230,[13]	85	32-bits	12						
Qualcomm Q2220 (3),[16]	50	24-bits	10						
Analog Devices AD7008,[17]	50	32-bits	10	no	12-bits	no			44-pin PLCC
Analog Devices (1) AD9720,[17]	250		10						Dip and LCC
Sandia,[18]	590	24-bits	8	yes	12-bits		GaAs		PWB
University of Bradford UK DDS,[19]	500	32-bits	8				GaAs		
TMC2340 w/ TDC1012,[20]	20	32-bits	12	no	32-bits	yes	CMOS/ bipolar		
DAC Triquent SC-0806-C,(1)[21]	1000		14						
Burr-Brown, (1) DAC600,[22]	256		12				Bipolar		
HP(1),[23]	1000		12				GaAs		
AD9830[17]	50	32-bit	10	no	yes	no	CMOS	250Mw	48-pin TQFP
DAC Rockwell,(1)[24]	1000		12				SiGe HBT		
DAC Rockwell (1) RI61008 [25]	1200		10				GaAs		

Some surveyed wideband DACs do not show up on the survey chart in figure 9 because no published data on the spurious performance was determined. However, they are of particular interest because of the high clock rate or novel architecture. For example, Rockwell has reported development of a 12-bit, 3-GHz DAC [Loring,1994]. For novel DAC architectures, see [Takakura et al., 1991], [Hawksford, 1994], [Kim, 1993], [Essenwanger, 1998], and others listed in the references and bibliography. An example of a high-speed DDS/DAC is the Raytheon IC and module design shown in figures 10 through 14.

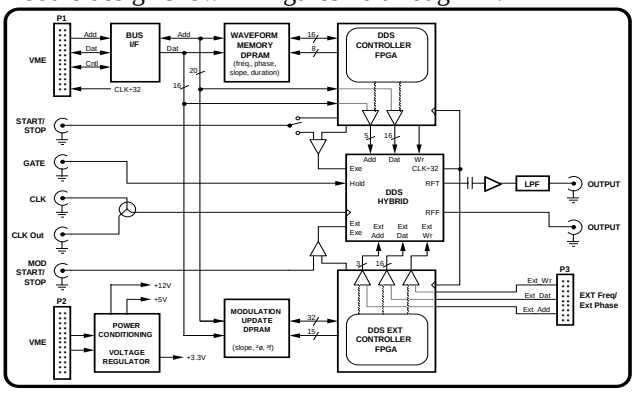

Figure 10. Block Diagram of Raytheon DDS Module[2].

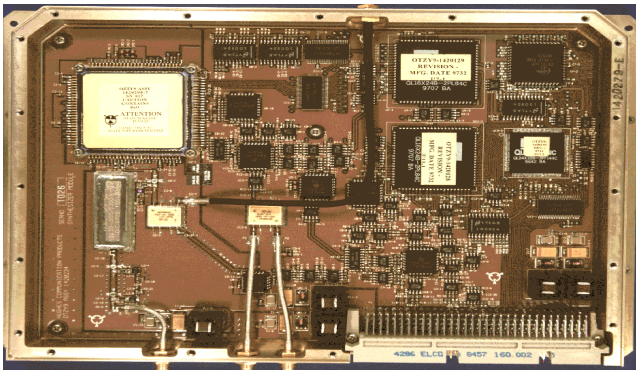

Figure 11. Photograph of the Raytheon DDS Module.

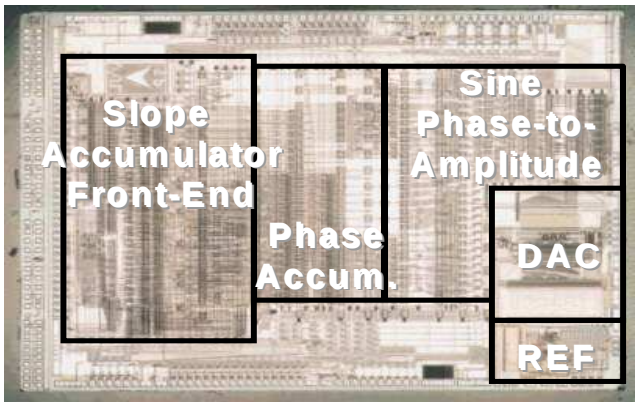

Figure 12. The Raytheon IC chip.

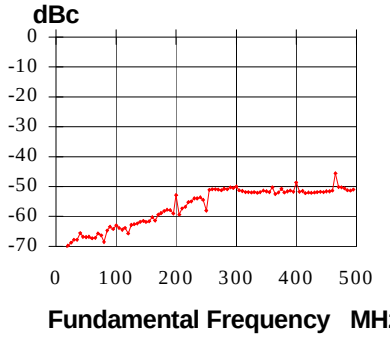

Figure 13. Typical worst case spurious performance of the Raytheon DDS/DAC module [2].

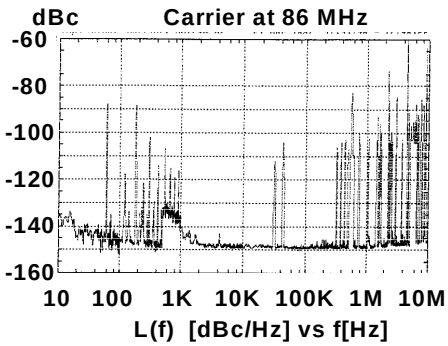

Figure 14. Measured phase noise for the Raytheon DDS/DAC [2].

Conclusions

There are major challenges in DDS designs, particularly in the DAC, to achieve the design goal of about –90dBc SFDR and GHz clock rates for wideband output capability. The technology needed to achieve this goal, through the use of advanced IC process technology and novel circuits, was presented. The survey revealed a barrier in performance attributed primarily to the dynamic imperfections of high speed DACs. Standardization in the specification and measurement of spurious performance is also needed.

References and Bibliography

Survey Chart References

1. Zavrel, Robert J., Jr. and Edwards, Gwyn; Editors; The DDS Handbook. Second Edition, Stanford Telecommunications, Inc., Custom & ASIC Products Group. July, 1990.

2. Data Sheet RAP 1420830. "1 GHz DDS Module." Raytheon Systems Company, Raytheon Advanced Products, Torrance, CA, 1998.

3. Plessey Data Book, Professional Products IC Handbook, GEC Plessey Semiconductors, June 1994.

4. Kent, Gary W.; Sheng, Neng-Haung; "A High Purity, High Speed Direct Digital Synthesizer." 1995 IEEE Frequency Control Symposium.

5. Kushner, Lawrence J.; Ainsworth, Marcus T.; "A Spurious Reduction Technique for High-Speed Direct Digital Synthesizers", Lincoln Laboratory, Massachusetts Institute of Technology. IEEE International Frequency Control Symposium, 1996, pp 920-927.

6. Andrews, G. Van; Chang, C. T. M.; Cayo, S. S.; White, W. A..; Harris, M. P.; "A Monolithic Digital Chirp Synthesizer Chip with I and Q Channels.' Texas Instruments Inc.,1991 IEEE GaAs IC Symposium, March 91, pp. 19-22.

7. Sciteq Data Book, “Frequency Synthesis & RF Subsystems.” Sciteq Electronics, Inc., 1994.

8. Schaffer, T. A.; Warren, H. P.; Bustamante, M. J., and Kong, K. W., "A 2 GHz 12-bit Digital-to-Analog Converter for Direct Digital Synthesis Applications." Hughes Space and Communications, 1996 IEEE GaAs IC Symposium, pp. 61-64.

9. Private telephone conversation between Victor Reinhardt and Mario Bustamante, May, 1998.

10. CAGLIO, Nathalie; DEGOUY, Jean-Luc; MEIGNANT, Didier; ROUSSEAU, Patrick; LEROUX, Bruno; "An Integrated GaAs 1.25 GHz Clock Frequency FM-CW Direct Digital Synthesizer." LEP/Philips Microwave Limeil, Thomson CNI, 1993 IEEE, GaAs IC Symposium, pp167-170.

11. Sharma, Arvind K.-Chairman,"Direct Digital Synthesis and TRW Custom HBT Chips." 1995 IEEE, International Microwave Symposium, Workshop WFFD: Advances in Microwave and mm-Wave Synthesizer Technology, May 19, 1995. Orlando, Florida

12. Tan, Loke K.; Roth, Edward; Yee, Gordon E.; Samueli, Henry; "An 800MHz Quadrature Digital Synthesizer with ECL-Compatible Output Drivers in 0.8µm CMOS." Broadcom Corporation, 1995 IEEE International Solid-State Circuits Conference, paper FA 15.1, pp258-259,198-199.

13. Qualcomm Data Book; "Master Selection Guide." Qualcomm VLSI Products, 80-3751 C, June, 1995.

14. Qualcomm Data Book; "Q2334 Dual Direct Digital Synthesizer." Qualcomm Inc., DL90-2334C, May 1995.

15. Hill, Allen; and Surber, Jim; "Using Aliased-Imaging Techniques in DDS to Generate RF Signals." RF Design, Sept. 1993.

16. Qualcomm Data Book; "Q2220 Direct Digital Synthesizer." Qualcomm Inc., DL80-3749-1C, Aug. 1993.

17. G2132-150-5/96, Designer's Reference Manual, Data Converters." Analog Devvices Inc., 1996.

18. Remund, Brett L.; Srivatsa, Charkra R., "A 500 MHZ PHASE GENERATOR FOR SYNTHETIC APERTURE RADAR WAVEFORM SYNTHESIZERS", Sandia National Laboratories, GaAs IC Symposium, IEEE 1991. Pp 349-352.

19. Benn, H.P.; Jones, W.J.; "A Fast Hopping Frequency Synthesizer." University of Bradford UK,IEE Conference Pub. #303 2nd International Conference on Frequency Control and Synthesis, 1989, pp 10-13.

20. --.1994 DATA BOOK, Raytheon Semiconductor (Previously TRW LSI Products).

21. Data Sheet SC-0806-C. "1GS/s 14 Bit Digital to Analog Converter", TriQuent Semiconductor, Oct 1,94.

22. FAX, Burr-Brown Mktg, DAC600, "12-Bit 256Mhz Monolithic Digital-to-Analog Converter", PDS1153 Data Sheet, Bur-Brown Corporation, Sept. 9. 1992.

23. Hsieh, Kuo-Chiang; Knotts, Thomas A.; Baldwin, Gary L.; Hornak, Thomas, " A 12-bit 1-Gword/s GaAs Digital-to-Analog Converter System." IEEE Journal of Solid-State Circuits, Vol. SC-22, NO. 6, Dec. 1987.

24. Goodenough, F., *12-Bit DAC Runs at 1 Ghz, Puts 20 mA Into 50 (Ohms*), Electronic Design, pp 47-52, February 7, 1994.

25. Wirbel, Loring;"1.2-GHz GaAs D/A set." EE Times, June 6, 94.

DDS Spurious Theory References and Bibliography

26. Sunderland, D.A., et al., *CMOS/SOS Frequency Synthesizer LSI Circuit for Spread Spectrum Communications*, IEEE Journal of Solid-State Circuits Vol. SC-19, No. 4, pp 497-506, August 1984.

27. Essenwanger, K.A., *Spurious Suppression in Direct Digital Frequency Synthesis by Combined Dithered Accumulator and Sine Approximation Techniques*, Masters Thesis, Cal Poly, Pomona, May 1987.

28. J. F. Garvey and D. Babitch, "An Exact Analysis of a Number controlled Oscillator Synthesizer," IEEE Frequency Control Symposium, 1990.

29. G. C. Gillette, "Digiphase Principle," Frequency Technology, August, 1969.

30. V. S. Reinhardt, "Direct Digital Synthesizers," Proceedings of the 17th NASA/DOD PTTI Planning Meeting, Washington, D C., Dec., 1985.

31. Estrick, Vaughn and Essenwanger, K. A.; "Direct Digital Synthesizer Survey." an internal for the RF Systems Technology Network (RFSTN) at Hughes Aircraft now known as Raytheon Systems Company, Nov. 8, 1995.

32. Tierney, Joseph, Rader, Charles M., and Gold, Bernard. “A Digital Frequency Synthesizer”, IEEE Transactions on Audio and Electroacoustics. Vol. Au-19. No. 1. March 1971. 48-57.

33. Nicholas, H.T. III, and Samueli H., Kim, B., *The Optimization of Direct Digital Frequency Synthesizer Performance in the Presence of Finite Word Length Effects*, IEEE Annual Frequency Control Symposium, pp. 357-363, 1988.

34. Nicholas, H.T. III, and Samueli H., *An Analysis of the Output Spectrum of Direct Digital Frequency Synthesizers in the Presence of Phase-Accumulator Truncation*, IEEE 41st Annual Frequency Control Symposium, pp. 495-502, 1987.

35. O’Leary, P., and Maloberti, F.; “A Direct-Digital Synthesizer with Improved Spectral Performance.” IEEE Trans. on Comm. Vol. 39, No. 7, July 1991.

36. Flanagan, M. J., and Zimmerman, G. A.; “Spur-Reduced Digital Sinusoid Synthesis.” IEEE Trans. on Comm. Vol. 43, No. 7, July 1995, pp. 2254-2262.

37. Vankka, J.; “Spur Reduction Techniques in Sine Output Direct Digital Synthesis.” 1996 IEEE International Frequency Control Symposium, pp. 951-959.

38. Karlquist, R. K.; “A 3 to 30 Mhz High-Resolution Synthesizer Consisting of A DDS, Divide-and-Mix Modules, and a M/N Synthesizer.” 1996 IEEE International Frequency Control Symposium, pp. 928-933.

39. Vankka, J., Waltri, M., Kosunen, M., and Halonen, K. A. I.; “A Direct Digital Synthesizer with an On-Chip D/A-Converter.” IEEE Journal of Solid-State Circuits, Vol. 33, No. 2, Feb. 1998. pp. 218-227.

DAC References and Bibliography

40. Colotti, J. J.; “Dynamic Evaluation of High Speed, High Resolution D/A Converters.” RF Design, 1990, pp. 51-64

41. Essenwanger, K. A, “Slewer Fractional-Order-Hold: The Ideal DAC Response for Direct Digital Synthesizers.” The 1998 IEEE International Frequency Control Symposium, May 1998.

42. Essenwanger, K. A.; “Final Report Evaluation of Digital-to-Analog Converters…” under contract to Hughes Space and Communications, Sept. 13, 1996.

43. Takkura, H.; Yokoyama, M.; and Yamaguchi, A.; “A 10 bit 80MHz Glitchless CMOS D/A Converter.” IEEE 1991 Custom Integrated Circuits Conference, pp. 26.5.1-26.5.4.

44. Hawksford, M. A.; “Digital-to-Analog Converter with Low Intersample Transition Distortion and Low Sensitivity to Sample Jitter and Transresistance Amplifier Slew Rate.” J. Audio Eng. Soc., Vol. 42, No. 11, Nov. 1994, pp. 901-916.

45. Kim, O., et al., *Settling Time Reduction Technique for High Speed DACs*, Electronics Letters, Vol. 29, No. 25, Dec. 9, 1993, pp. 2191-2192.

46. Mercer, D., A 16-bit Converter with Increased Spurious Free Dynamic Range, IEEE Journal of Solid-State Circuits, Vol. 29, No. 10, Oct. 1994.

47. Nakamura, Y., et. al., A 10-b 70-MS/s CMOS D/A Converter, IEEE Journal of Solid-State Circuits. Vol. 26, No. 4., pp. 637-642, April 1991.

48. Jensen, H T., and Galton, I.; “A Low-Complexity Dynamic Element Matching DAC for Direct Digital Synthesis.” IEEE Trans. on Circuits and Systems—II, Vol. 45. No.1, Jan. 1998.

49. Spang, H. A. III; “Reduction of Quantizing Noise by Use of Feedback.” IRE Trans. on Comm. Syst. Vol. CS-10, pp 373-380, Dec. 1962. (reprinted in Waveform Quantization and Coding. Jayant N. S. Editor, IEEE Press, 1976).

50. Chen, F., and Leung, B.; “A Mulit-Bit ΣΔ DAC with Dynamic Element Matching Techniques.” IEEE 1992 Custom Integrated Circuits Conference, pp 16.2.1-16.2.4.

51. Rabiner, L.R. and Gold B.; Theory and Application of Digital Signal Processing. Prentice-Hall, Englewood Cliffs, N.J. 1975, p. 330.

52. Benz, S. P.; Hamilton, C. A.; Burroughs, Jr. C. J.; Harvey, T. E.; Christian, L. A.; and Przybysz, J. X.; “Pulse-Driven Josephson Digital/Analog Converter.” IEEE Transactions on Applied Superconductivity, Vol. 8, No.2, June 1998, pp. 42-47.

IC Process References and Bibliography

53. Eason, S. D.; “SiGe Stretches Limits of Silicon Applications.” Microwaves & RF, Dec. 1996, pp89-96.