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SPUR REDUCTION TECHNIQUES IN DIRECT DIGITAL SYNTHESIZERS

Victor S. Reinhardt
Hughes Space and Communications Company
P. O. Box 92919, Los Angeles, California 90009

Abstract

This paper reviews spur reduction techniques used in direct digital synthesizers (DDSs) or numerically controlled oscillators (NCOs). First, the classification and operation of conventional DDSs are reviewed. Covered are the pulse output DDS, sine output DDS, fractional divider, and phase interpolation DDS. It is shown that DDSs produce spurs as well as the desired output frequency due to the aliasing of harmonic imperfections in the generated waveform. Next, spur reduction techniques which reduce spurs by destroying the coherence of the aliasing process are discussed. Architectures described are the spurless fractional divider, the Wheatley jitter injection DDS, the randomized DAC DDS, and the nonuniform clock DDS. The spur reduction and phase jitter properties of each architecture are also discussed.

Introduction/Review of DDSs

Direct digital synthesizers (DDSs) or numerically controlled oscillators (NCOs) directly synthesize frequency waveforms from a fixed reference frequency using digital waveform generation techniques. DDSs can be classified as the pulse output DDS, sine output DDS, fractional divider, phase interpolation DDS, and other minor DDS variations [1]. The major classifications are summarized below. For more detailed descriptions, see References 1, 2, 3, 4, 5, and 6.

Pulse Output DDS

Figure 1 shows a block diagram of the pulse output DDS and outlines its operation. The pulse output DDS merely consists of an N-bit accumulator set up to add a frequency word K every clock cycle t_c or

$$R_{n+1} = \mathrm{Mod}(R_n + K, 2^N) \quad (1)$$

where R_n is the N-bit register value in the accumulator after the nth clock cycle. One can take the frequency output f_o from the carry output as a pulse or from the most significant bit (MSB) of the accumulator as a "square" wave. From the figure, one can see that on average

$$f_o = F_o f_c \quad (2)$$

where F_o the fractional frequency is

$$F_o = \frac{K}{2^N} \quad (3)$$

and where the clock frequency f_c is $1/t_c$.

The main limitation of the pulse output DDS is the high degree of time or phase jitter it exhibits. One can see from Figure 1, that the time error between the actual zero crossings of the output and that of an ideal frequency source varies approximately uniformly from 0 to t_c. This produces a time jitter of

$$\sigma_t \cong \frac{t_c}{2\sqrt{3}} \quad (4)$$

Let us define a fractional register value

$$r_{n+1} = r_n + F_o \quad (5)$$

which is related to the accumulator register word R_n by

$$\mathrm{Fract}(r_n) = \frac{R_n}{2^N} \quad (6)$$

One can see from Figure 1 that, at sample time nt_c, r_n is equal to the cycle count elapsed in an ideal oscillator with frequency f_o. Thus the elapsed phase is

$$\phi = 2\pi r_n \quad (7)$$

and the value of R_n at a carry is proportional to the phase error of the output pulse. (This will be important in other DDS designs.) Finally, from (4) and Figure 1, one can see that the phase jitter of the unfiltered output is given by

$$\sigma_\phi \cong \frac{\pi F_o}{\sqrt{3}} \quad (8)$$

The filtered jitter is a completely different matter. Figure 2 shows a typical plot of the spectrum from a pulse output DDS. Notice the dense collection of large spurs around the carrier due to aliasing. The character and position of these spurs change drastically as f_o is changed. Because large aliasing spurs, which contain large amounts of jitter energy, can appear very close to the carrier at certain frequencies, one cannot reliably improve the phase jitter of a pulse output DDS by filtering. This problem is corrected by the spur reduction techniques discussed later.

Sine Output DDS

The sine output DDS reduces the phase jitter of the pulse output DDS by adding a sine look-up table and digital to analog converter (DAC or D/A converter) to the N-bit accumulator as shown in Figure 3. In this DDS, The N-bit accumulator register provides a W-bit phase word for a J-bit sine look-up table, whose output is converted to an analog voltage by an M-bit DAC. An example of the resultant stepped DDS output is also shown in Figure 3.

If the sine output voltage is perfect, using the sampling theorem [7], one can show that a pure sine wave at f_o will be recovered when the output is low-pass filtered with a cut-off frequency below $f_c/2$. When the look-up table and DAC have finite resolution, spurs will be generated [1,3,9,10]. Generally, DAC quantization is the limiting factor in sine output DDSs. A rough order of magnitude for the size of spur levels (power) is 2^{-2M}, but other analysis has shown that the dependence on DAC resolution M is faster than this when the sine table has a much higher resolution than the DAC [9,10]. Figure 4 shows typical sine output DDS frequency spectrums with 5-bit and 11-bit DACs.

Fractional Divider and Phase Interpolation DDS

The fractional divider or pulse swallower shown in Figure 5 is similar in operation to the pulse output DDS. In the fractional divider, a programmable divide by n/n+1 counter normally divides clock cycles by n. At each divide output, an N-bit accumulator is clocked to add the frequency word K to itself. Whenever there is a carry, the next divide cycle is then set for divide by n+1. One can show that this produces an output whose average frequency is given by [1]

$$f_o = \frac{f_c}{n + F_o} \quad (9)$$

The fractional divider, like the pulse output DDS, produces a high degree of jitter. The phase interpolation DDS shown in Figure 6, like the sine output DDS, reduces this jitter. As shown in the figure, the fractional divider is used in a phase lock loop. This inverts the fractional division process, so the output is

$$f_o = (n + F_o) f_c \quad (10)$$

Since the register value R_n is proportional to the phase error of the fractional divider output [1], its value is used to provide a phase correction to the loop through a DAC. Like the sine output DDS, the spurs are roughly given by 2^{-2M} for an M-bit DAC. The main disadvantage of the phase interpolation DDS is that M-bit linearity and accuracy are also required of the phase detector.

Theory of Conventional DDS Spurs

To simplify the derivations that follow, let us use normalized time and frequency units given by

$$F = f/f_c = f\, t_c \quad (11)$$

$$T = t/t_c = t\, f_c \quad (12)$$

Figure 7 shows the DDS model we will use. The first block in the model is a look-up table v(r). This look-up table uses the normalized register value r to generate a voltage v. An important property of v(r) is that it is periodic in r with a period of one; that is, the look-up table only utilizes the fractional part of r to generate voltage values.

The next block in our model is an accumulator which generates a sequence of normalized register values r_n and samples of v(r) given in the time domain by

$$v_s(T) = \sum_n v(r_n)\delta(T - n) \quad (12)$$

The final block in our model is a hold function given by

$$h(t) = \begin{cases} 1 & \text{if } -1/2 < T < 1/2 \\ 0 & \text{otherwise} \end{cases} \quad (13)$$

which generates the stepped DDS output given by

$$v_h(T) = \int h(T-T')\, v_s(T')\, dT' \quad (14)$$

This model can be applied to both pulse output and sine output DDSs. For the pulse output DDS, v(r) is a square wave, and for the sine output DDS, v(r) is a quantized sine wave. The fractional divider and phase interpolation DDSs, can also be understood by suitably modifying the model.

Fourier Transform of DDS Output.

The fourier transform of the DDS output $V_h(F)$ is then given in terms of the fourier transform of the sampled signal $V_S(F)$ and the fourier transform of the hold function H(F)

$$V_h(F) = V_S(F) \cdot H(F) \quad (15)$$

where

$$V_h(F) = \int_{-\infty}^{\infty} v_h(T) e^{-j2\pi FT} dT \quad (16)$$

$$H(F) = \mathrm{Sinc}(\pi F) \quad (17)$$

and

$$V_S(F) = \sum_n v(r_n) e^{-j2\pi nF} \quad (18)$$

Because of the normalized units, note that all fourier transforms and spectral densities are per f_c Hertz. Thus to obtain per Hz formulas, one must divide frequency domain formulas in this paper by f_c and substitute f_o/f_c and f/f_c for F_o and F respectively.

Since v(r) is periodic with an r-period of one, we can expand v(r) as a fourier series [10]

$$v(r) = \sum_m a_m e^{j2\pi mr} \quad (19)$$

Thus (18) becomes

$$V_S(F) = \sum_{m,n} a_m e^{j2\pi(mr_n - nF)} \quad (20)$$

Spurs in a Conventional DDS

In a conventional DDS

$$r_n = F_o n \quad (21)$$

so from (20), V_S is given by

$$V_S(F) = \sum_{m,n} a_m e^{j2\pi F_m n} \quad (22)$$

where

$$F_m = mF_o - F \quad (23)$$

Utilizing the well known aliasing relationship for sampled signals [1,7]

$$\sum_{n=-\infty}^{\infty} e^{j2\pi nF} = \sum_{m'=-\infty}^{\infty} \delta(F - m') \quad (24)$$

we obtain

$$V_S(F) = \sum_m a_m \sum_{m'(m)} \delta(F - F_{m,m'}) \quad (25)$$

where

$$F_{m,m'} = mF_o - m' \quad (26)$$

Thus one obtains the well known fact that sampling produces aliasing [7]; that is, the harmonics of $v(F_o t)$ at $f=mf_o$ are aliased down to spurs by multiples of the clock frequency

$$f_{m,m'} = mf_o - m'f_c \quad (27)$$

The frequencies of DDS spurs can be predicted using (27). It can be shown [1] that the spur frequencies $F_{m,m'}$ are given by a permutation of 1/b, 2/b, ..., (b-1)/b where F_o is written as the simplified fraction a/b (a and b relatively prime to each other). The size of these spurs can also be predicted by calculating the a_m. For a pulse output DDS, the a_m are the harmonics of a square wave [3,7]. For a sine output DDS, the evaluations of a_m for the quantized sine wave have also been published using analytical techniques [8] and computer simulations [9].

Spur Reduction Techniques

As described in the previous section, spurs occur in a DDS because of aliasing from the uniformly stepped periodic (period = $N't_c$) sequences generated. In the following sections we will discuss methods of reducing these spurs by destroying the periodicity of these sequences. Table 1 summarizes spurs reduction techniques in the literature. The last technique by Nicholas and

Samueli [16] does not involve destroying the periodicity of the DDS steps and will not be discussed.

Table 1. Spur reduction techniques.

Technique	Refer-ence	Method
Spurless Fractional Divider	[11]	Totally Random Output
Wheatley Jitter Injection	[12] [13]	Word Jitter Injection
Randomized DAC DDS	[14]	Word Jitter Injection
Nonuniform Clock DDS	[15]	Nonuniform Sampling
Nicholas & Samueli DDS	[16]	Force K to Be Odd

Spurless Fractional Divider

Figure 8 shows a block diagram of a spurless fractional divider [11]. This consists of a programmable divide by n/n+1 counter, an N-bit random or pseudorandom number generator, and an N-bit word comparator. At every output of the divider, the random number generator produces a new random word P_n, and the comparator compares this word with the frequency word K. If $P_n<K$, the counter is set to divide by n+1 for the next cycle. On average, the frequency will be given by (9) just as for the conventional fractional divider, but the sequence of divide by n's and n+1's will be totally random, so no spurs will be generated. However, this process generates frequency jitter, so the spurless fractional divider has a $1/f^2$ phase noise spectrum near the carrier.

Wheatley Jitter Injection DDS

Figure 9 shows one form of the Wheatley jitter injection DDS [12,13]. In this variation on a pulse output DDS, a random word k_n, which can vary randomly from 0 to K-1, is generated each clock cycle and added to the accumulator register value R_n. The sequence of carries from this addition then becomes the pulse output. In the original Wheatley circuit, this output is also divided by two to produce a "square" wave. Figure 10 shows the spectrum of a pulse output DDS with and without Wheatley jitter injection. Notice that the Wheatley DDS quite effectively removes most spurs, but trades these spurs for a high degree of broadband phase noise S_ϕ. In essence, the phase jitter of the pulse output DDS is still there, but now smeared out into broadband noise. This broadband noise is more easily filtered out than spurs; now the filtered phase jitter is just $\sqrt{S_\phi B}$ where B is the filter noise bandwidth (B assumed to be small).

One can show that the spur power at $F_{m,m'}$ in the Wheatley jitter injection DDS is smaller than that in a pulse output DDS by a factor of [1]

$$|M|^2 = \mathrm{Sinc}^2(\pi m F_o) \qquad (28)$$

Notice that only m, the order of the original harmonic expansion of v(r), matters in reducing spurs, not the final frequency $F_{m,m'}$. Thus spurs which come from low order harmonics are not completely eliminated by the jitter injection process.

Several formulas have been published for the spectral density of the noise floor [1,12,13]. These have the same dependence on the basic parameters f_o and f_c, but have different coefficients.

Randomized DAC DDS

The comparable jitter injection technique for sine output and phase interpolation DDSs is the randomized DAC DDS [14]. Figure 11 shows its sine output embodiment. Here a random word from 0 to $2^{J-M}-1$ is added to the J bit output of the sine look-up table before the sum is truncated to M bits for the DAC.

Figure 12 shows the spectrum of a randomized DAC DDS with a 5-bit DAC and those of a conventional sine output DDS with 5-bit and 11-bit DACs. Comparing spur levels, one can see that the randomized DAC DDS levels are at least 10 dB lower than those of the conventional DDS with the same resolution DAC, and has spur levels comparable to those of the conventional DDS with an 11-bit DAC. Especially note that the persistent spur nearest carrier in both sine output DDS plots is gone in the Randomized DAC DDS plot.

A final note is that the f_o in Figure 12 was chosen to provide a worst case example. Since f_o is approximately 1/3 f_c, many of the spurs near f_o are aliases of low order harmonics (m = ±2, ±4, etc.). These are are difficult to remove with jitter injection. At other values of f_o, the experimental results were even better [14].

Nonuniform Clock DDS

Another way to reduce the periodicity which produces spurs is to randomly vary the time interval between DDS steps. Figure 13 shows a DDS which accomplishes this by stepping a sine output nonuniformly in time [15]. To achieve this nonuniform stepping, a pseudorandom clock generator produces a sequence of pseudorandomly varying time intervals Δt_n and generates alternate odd and even clock pulses based on this sequence. A ΔR calculator next generates an accumulator increment

$$\Delta R_n = K\Delta t_n \qquad (29)$$

and an accumulator adds this to itself to produce a sequence of register values R_n. These R_n values are then utilized by a sine table to produce a sequence of sine values. At this point the sequence is broken up into odd and even values. These are stored in a buffer and sent individually to odd and even DACs. Finally, the DACs are clocked by the odd and even clock pulses and a Ping-Pong switch combines both DAC outputs into a single stepped output.

The separation into odd and even DACs is required to give the DACs sufficient time to settle. To eliminate spurs, the sequence Δt_n must uniformly vary from 0 to $2t_c$ [15], so some values of Δt_n will be virtually zero. The odd and even separation guarantees that each DAC will have a time of at least t_c to settle.

At first glance, this nonuniform clock method should produce no broadband noise because the exact phase increment for the sine table is properly calculated. However, the method does produce a broadband noise floor [15].

Conclusions

The randomization techniques described are an effective way of reducing spurs with minimum added complexity. Of the methods discussed, the jitter injection techniques--the Wheatley technique for the pulse output DDS and the randomized DAC DDS for the sine output and phase interpolation DDS--offer the best combination of manageable added phase noise and minimum added complexity. These techniques are also useful in reducing spurs in the face of technological component limitations such as limited DAC resolution and excessive settling time at high speeds.

Acknowledgment

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Figures

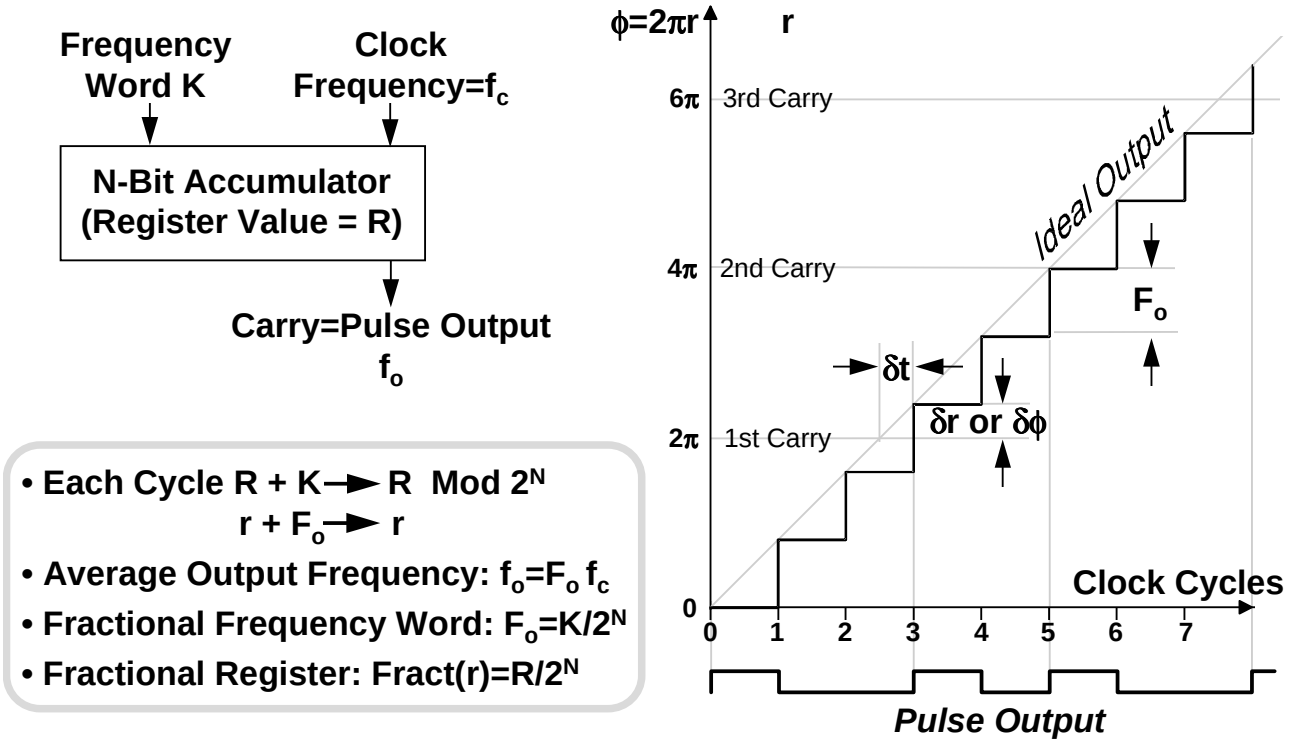

Figure 1. Pulse output DDS block diagram and operation.

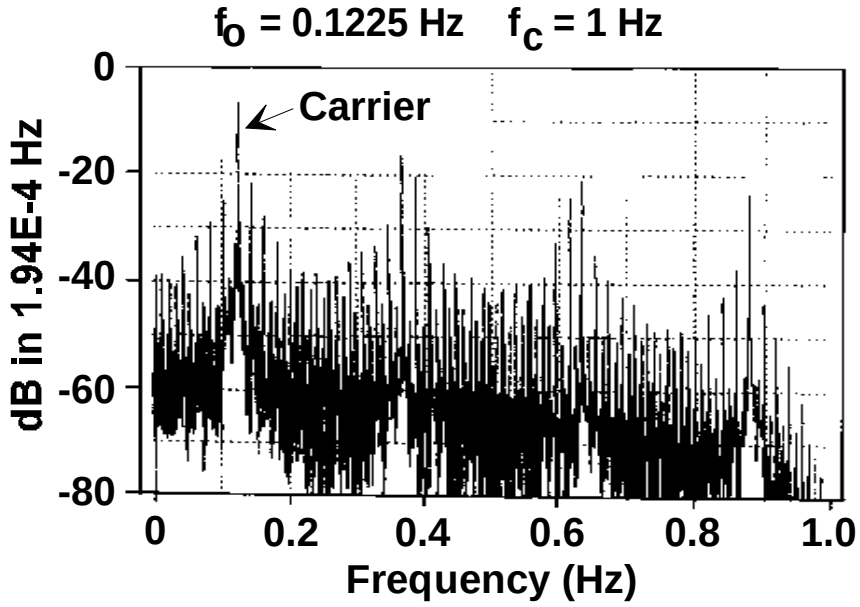

Figure 2. Typical pulse output DDS frequency spectrum.

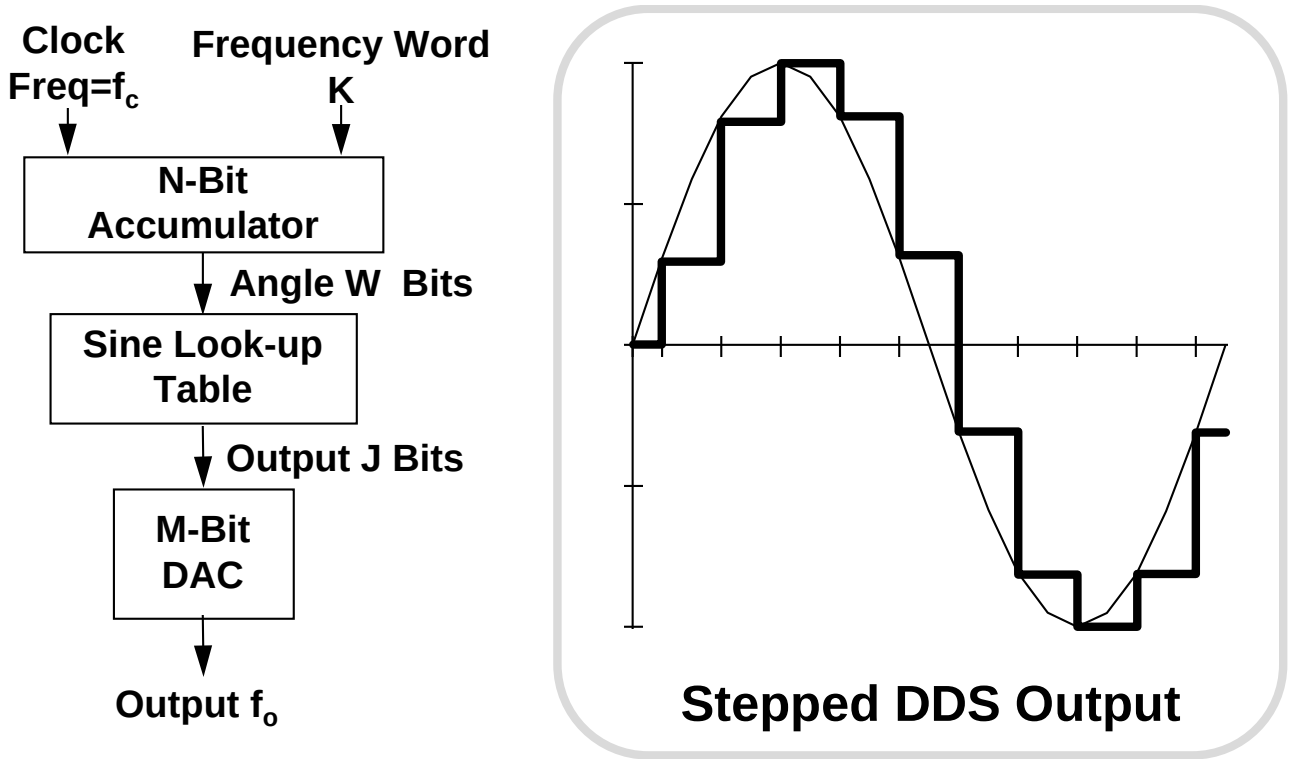

Figure 3. Sine output DDS block diagram and output waveform.

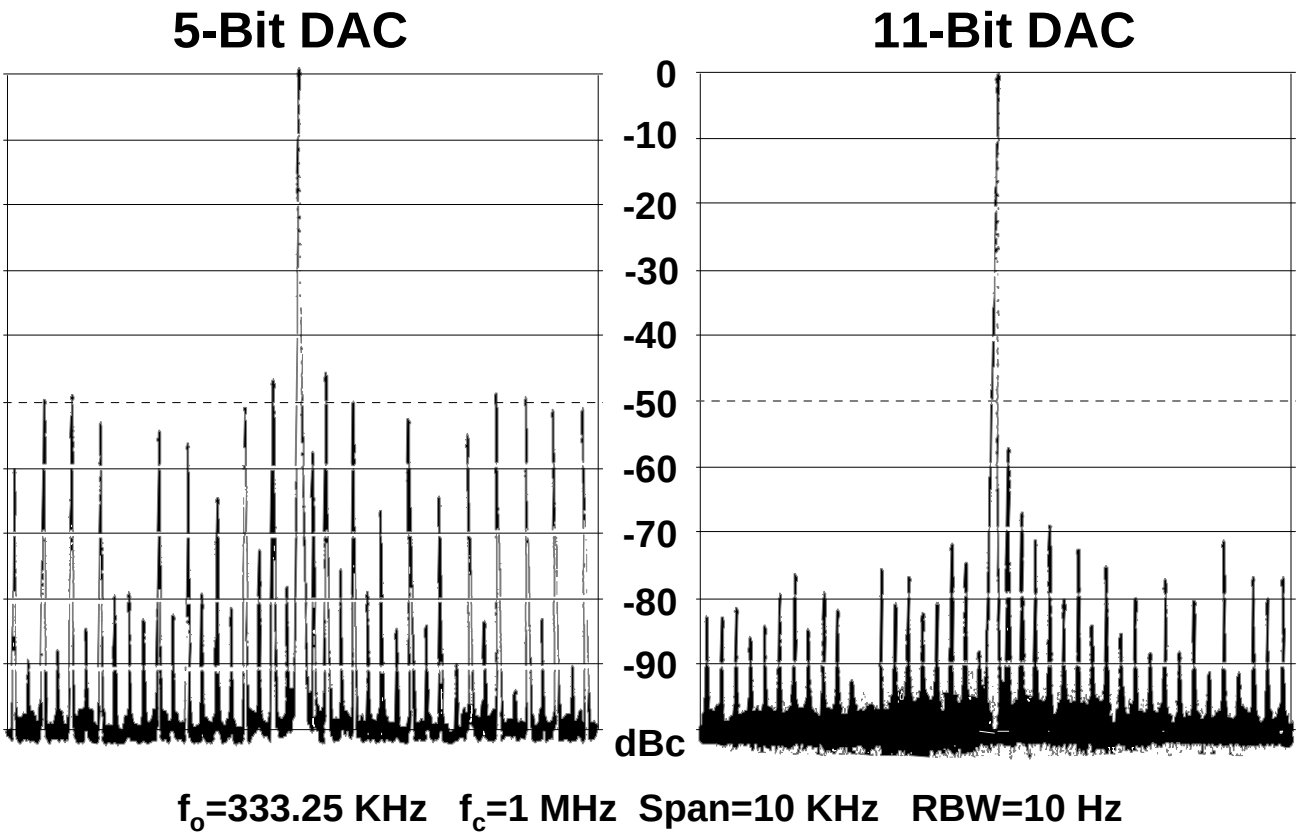

Figure 4. Typical sine output DDS frequency spectrum for 5-bit and 11-bit DACs

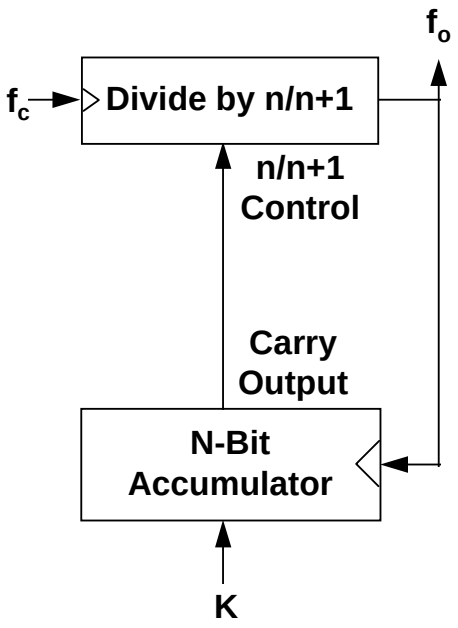

Figure 5. Fractional divider block diagram.

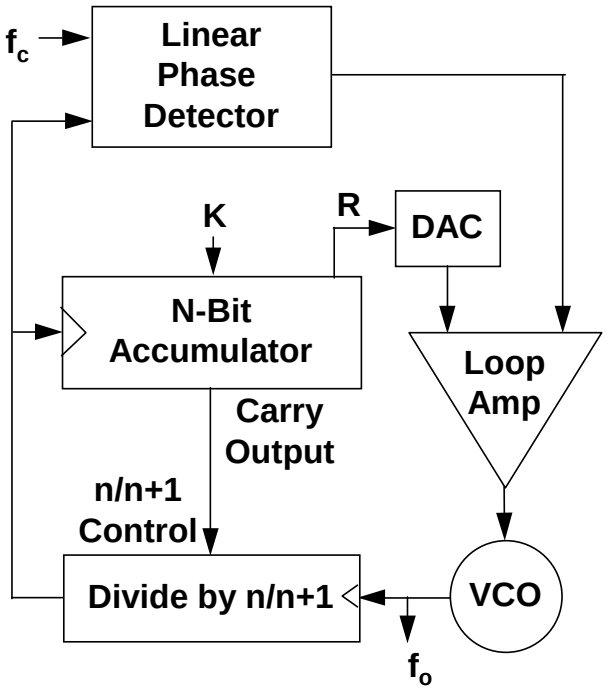

Figure 6. Phase interpolation DDS block diagram

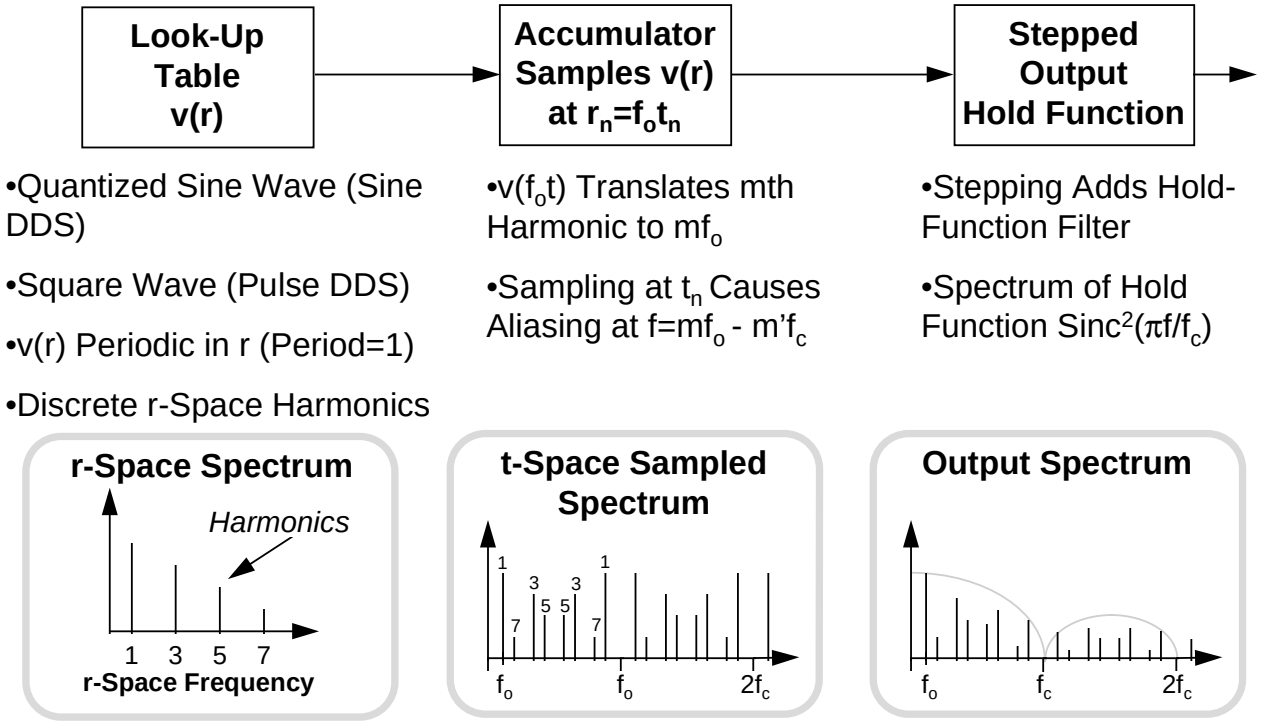

Figure 7. Model of uniformly sampled DDS and spur generation process.

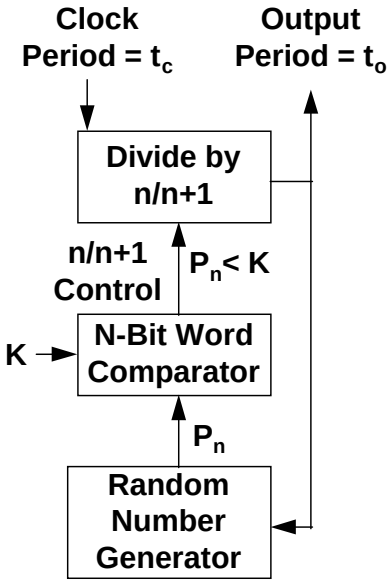

Figure 8. Spurless fractional divider block diagram

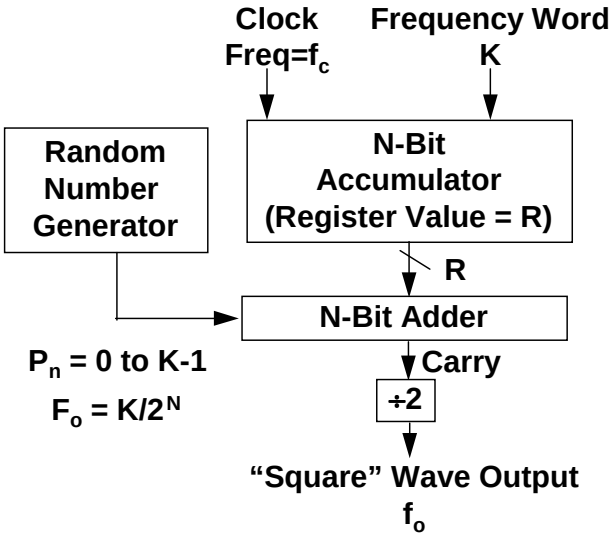

Figure 9. Wheatley Jitter injection DDS

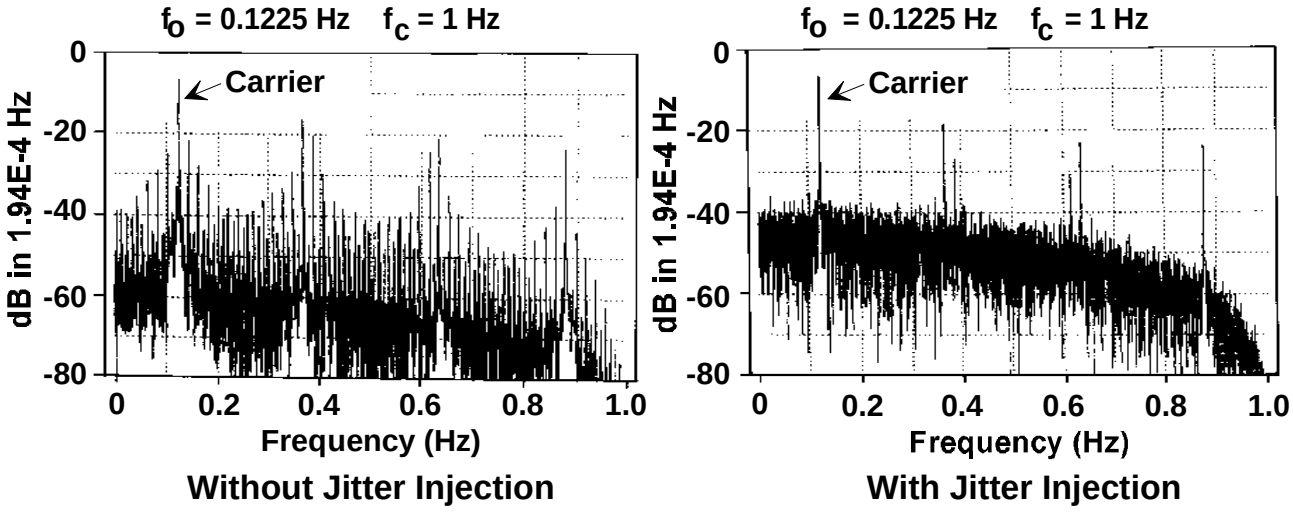

Figure 10. Wheatley jitter injection DDS frequency spectrum.

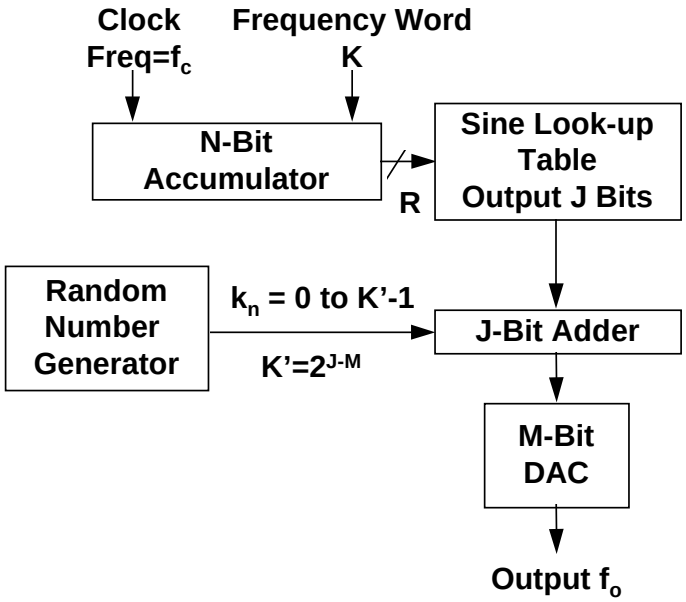

Figure 11. Randomized DAC DDS

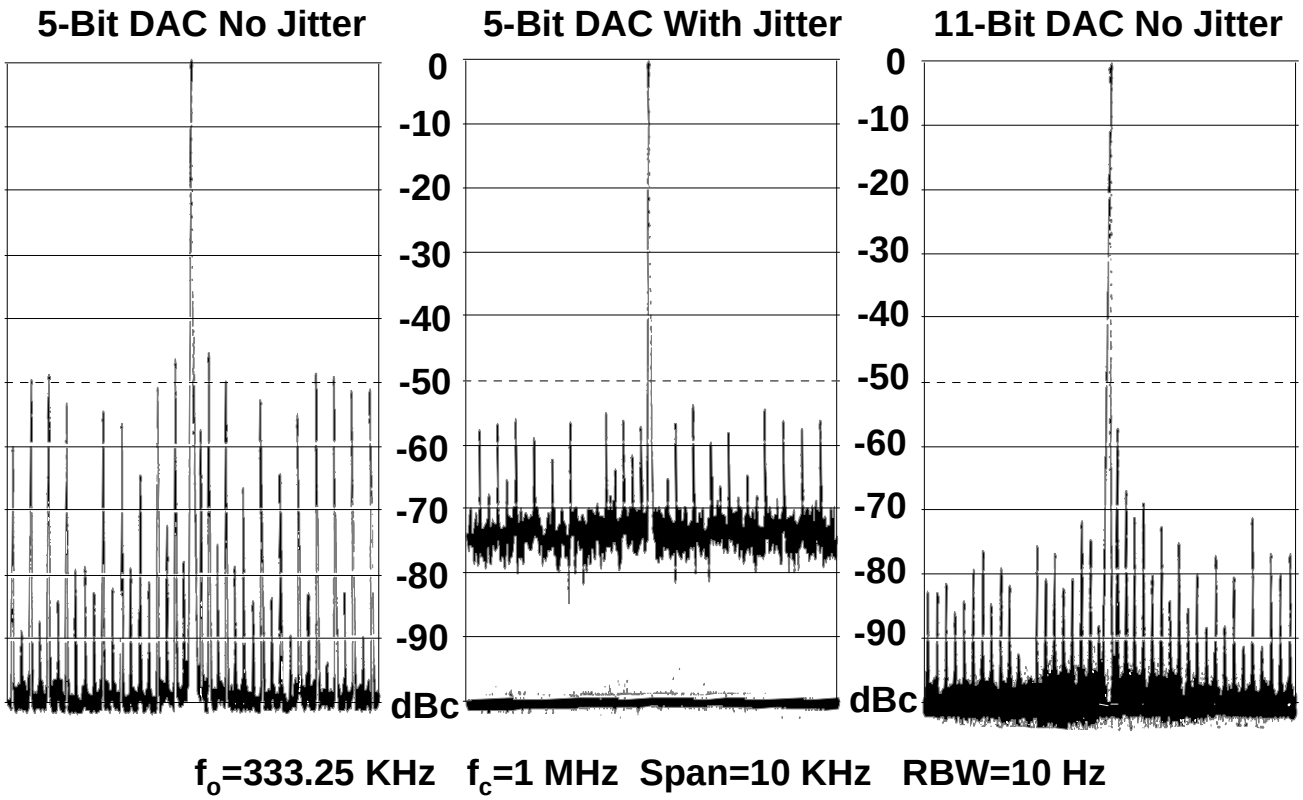

Figure 12. Comparison of Spectrums for sine output DDS and randomized DAC DDS.

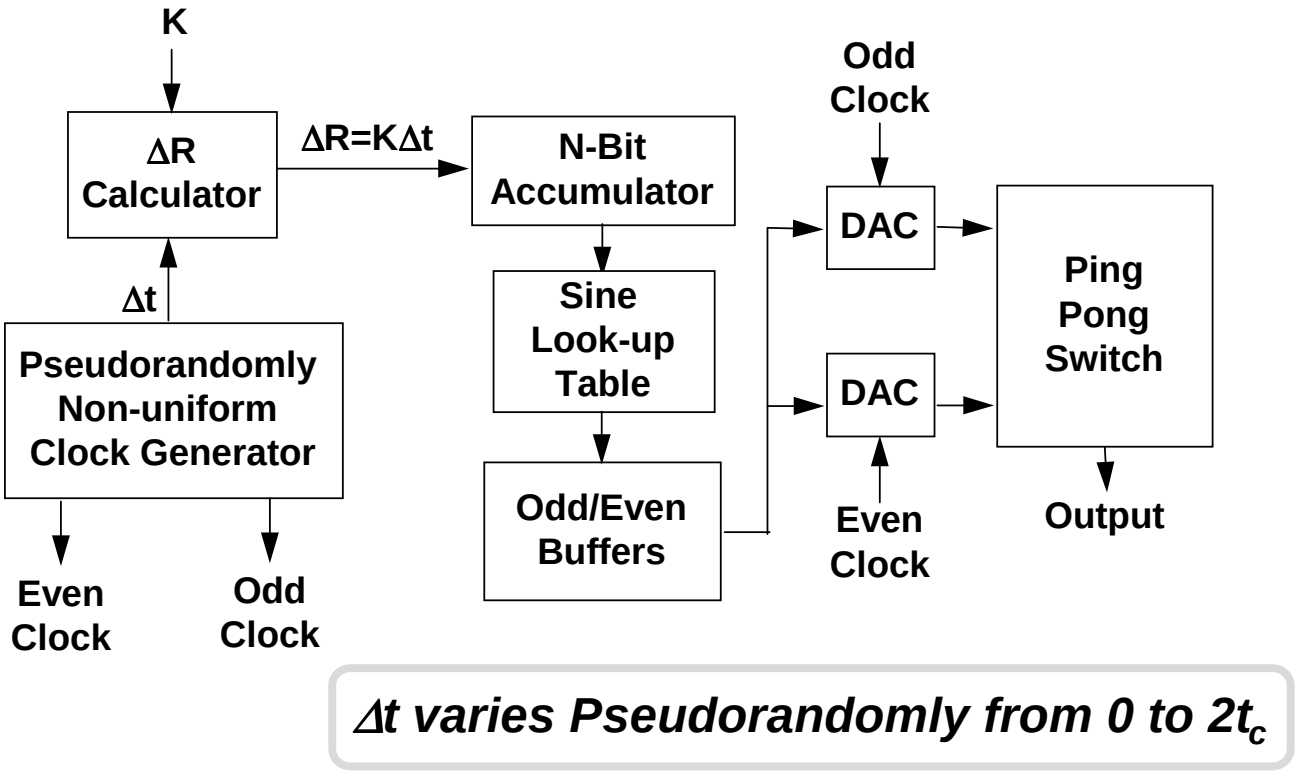

Figure 13. Nonuniform Clock DDS